



# HEVC 4K DECODER

Superior. Proven. Robust.

4KP60. 4:2:2. 12BITS.

## OVERVIEW

The HEVC 4K Decoder Core is a highly optimized video decompression engine targeted primarily at FPGAs. It is well suited for various applications ranging from broadcast and professional video to high end consumer electronics.

The decoder design is fully autonomous and does not require any external processor to aid the decode operation. The IO interface comprises of an input FIFO and an output frame buffer. Decoded data can also be provided on a serial bus with embedded sync information. The decoder requires DDR SDRAM to store reference pictures.

The decoder solution is available either as a FPGA netlist or in source code format and can be customized to meet the requirements of end users.

## KEY FEATURES

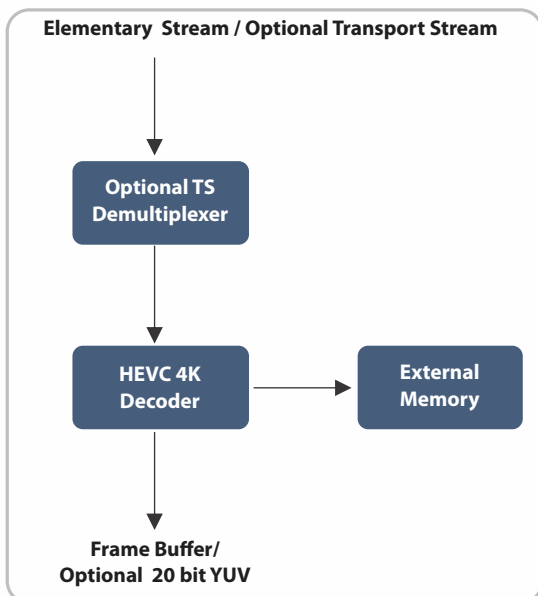
- Fully standards compliant - tested with ITU-T & other industry standard test suites.
- Robust error handling & resilience
- Processes metadata related to closed captions, AFD, timing & HDR
- Seamless switching between streams encoded with different settings including different resolutions, chroma formats and bit depths.
- Ultra-low latency
- Extensive options to customize the source code via use of parameters
- Single chip solution with no processor requirement
- Optimized resource utilization
- Easy to integrate

## FPGA RESOURCES

FPGA	LUTs	BRAMs	DSPs
Kintex Ultrascale	106,000	356	900

- 3840x2160p60, 422, 10-bit, 75 mbps decoder
- Does not include memory controller, display controller and TS demultiplexer

## BLOCK DIAGRAM



## SPECIFICATIONS

<b>Standard:</b>	HEVC/H.265 ( ISO/ IEC 23008-2 and ITU-T H.265 )
<b>Profiles:</b>	Main, Main10, Main 12, Main 10 4:2:2 and Main 12 4:2:2
<b>Video Resolutions:</b>	Up to 4096 x 2160
<b>Frame Rate:</b>	60 fps
<b>Bit rate:</b>	75 Mbps. Scalable to 150 Mbps
<b>Chroma Format:</b>	Monochrome, 4:2:0 & 4:2:2
<b>Precision:</b>	Bit depths from 8 to 12
<b>Input Format:</b>	Elementary or Transport stream
<b>Output Format:</b>	Decoded pictures in frame buffer. Optional serial output with embedded sync information
<b>Latency:</b>	As low as a few microseconds
<b>FPGA:</b>	Xilinx Kintex Ultrascale Arria-10 support coming soon

## DELIVERABLES

- Source Code or Netlist
- Simulation Model
- Hardware Test Platform
- Build Scripts
- Test Reports
- User Manual
- Design Documentation
- Constraint Files
- Test Benches
- Support for one year

## APPLICATIONS

### BROADCAST



### PROFESSIONAL VIDEO



### HIGH END CONSUMER ELECTRONICS



### AEROSPACE AND DEFENSE



### AUTOMOTIVE



### MEDICAL



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